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EXAMINER	
NGUYEN, CUONG QUANG	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/598,355	BASCERI ET AL.	
	Examiner	Art Unit	
	Cuong Q Nguyen	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25 and 51-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25, 51-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-6, 8-9, 11, 13-16, 18, 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunitomo et al. (US 6,235,572) in view of Summerfelt (US 5,622,893).

Regarding claims 1, 3-6, 8-9, 54, Kunimoto et al. discloses a semiconductor capacitor structure for storage charge comprising: a metallization layer (a contact plug structure including layer 30 and 49); a single conductive layer (54) formed directly on the metalization layer, the single conductive layer having a (second) compound (ruthenium oxide RuO) including a first substance (Ru) and a second substance (O) is formed by oxidized a Ru layer during crystallization of the tantalum oxide layer (61) (col.20 lines 63-67 and col.21 lines 1-15). Kunitomo et al. Further teaches that the morphology of the semiconductor structure remain stable during the crystallization process (col.20 lines 26-62); a single insulator layer (61, a tantalum oxide layer) formed directly on the single conductive layer, the single insulator layer having a first compound (tantalum oxide); a second conductive layer (62) formed directly on the single insulator layer, wherein the second conductive layer including a conductive portion (a portion of second conductive layer 62 extending on an upper surface of an insulating layer 46) formed below an upper surface of the single conductive layer. See Kunitomo et al.'s Fig.26 and Fig.26.

Kunitomo et al. does not explicitly teach that the single conductive layer further includes a trace amount of the first substance (ruthenium).

It is conventional and also taught by Summerfelt et al. (col.3 lines 43-55) that the single layer of capacitor electrode is formed by partially or fully oxidized the Ru still provides a stable conductive interface to the HDC material.

It would have been obvious to one of ordinary skill in the art to form the single conductive layer by partially oxidizing the Ru instead of fully oxidizing the Ru layer as taught by Summerfelt et al. because the single conductive layer being formed by both patrially or fully oxidizing Ru layer still provides a stable conductive interface to the HDC material.

It is noted that, the single conductive layer in the device being formed by the combination of Kunitomo et al. and Summerfelt et al. inherently includes a trace amount of the first substance (Ru). It is also noted that the second compound in Kunitomo et al. is identical as the second compound in the claims (ruthenium oxide). So, the second substance (oxygen) in Kunitomo et al. is inherently capable to prevent the oxygen (one substance of insulator layer) form the tantalum oxide (61).

Regarding claims 11, 13, 16, and 18 , Kunitomo et al. teaches that the lower capacitor electrode (54) being formed from the conductive layer (51, a ruthenium oxide RuO layer) before forming the insulator layer (61), therefore the lower electrode have been already oxidized when performing the high temperature crystallization processing of the tantalum oxide (61); the further oxidation of lower electrode is restricted and the leakage current of the tantalum oxide can be reduce. Kunitomo et al.'s col.21, lines 23-34.

It is noted that, the tantalum oxide having a permittivity value greater than about 25. See references US5177570, US5463483 and US5814539 which were cited to support the fact that tantalum oxide having a permittivity value greater than about 25.

Regarding claim 14, the crystallization processing of tantalum oxide layer is under a condition at temperature of 650 to 850 degrees Celsius (noted that a range 750 to 801 is in a range of 650 to 850). Kunitomo et al.'s col.19, lines 1-14.

Regarding claim 15, as discussed in the rejection of claim 11, the ruthenium oxide passivates the tantalum oxide from undesired oxidation of lower capacitor electrode layer (54).

Claims 1-25, 54-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 6,249,040) in view of Summerfelt et al. (US 5,622,893).

Regarding claims 1, 2, 3, 4, 5, 16, 17, 18, 19, 54, Lin et al. discloses a capacitor semiconductor structure for storing charges comprising: a metallization layer (a conductive plug162); a single conductive layer (165, a lower capacitor electrode of Ru) formed directly on the metallization layer; an insulator layer (166) formed directly on the single conductive layer, the insulator having a first compound of ditantalum pentaoxide (Ta_2O_5) having a crystalline structure of substantially (001) lattice plane and a permittivity greater than 25 (Lin et al.'s col.9, lines 25-37); a second conductive layer (169) formed directly on the single insulator layer, wherein the second conductive layer including a conductive portion (a portion of second conductive layer 169 extending on an upper surface of an insulating layer 159) formed below an upper surface of the single conductive layer. See Lin et al.'s Fig.10G.

Lin et al. does not explicitly teach that the single conductive layer includes a second compound of RuO_2 and a trace amount of Ru.

It is conventional and also taught by Summerfelt et al. (col.3 lines 43-55) that the single layer of capacitor electrode is formed by partially or fully oxidized the Ru in order to provide a stable conductive interface to the HDC material.

It would have been obvious to one of ordinary skill in the art to form the single conductive layer by partially oxidizing the Ru layer as taught by Summerfelt et al. because the single conductive layer being formed by both partially oxidizing Ru layer provides a stable conductive interface to the HDC material. col.3 lines 43-55

It is noted that, the single conductive layer in the device being formed by the combination of Lin et al. and Summerfelt et al. inherently includes a second compound (RuO_2) of a first substance (Ru) and a second substance (oxygen atoms), and a trace amount of Ru.

Regarding claims 6-15, Lin et al. teaches that the Ta2O5 capacitor insulator layer is annealing at temperature of 700-850 °C which in temperature range as claimed, so the capacitor insulator layer is inherently being crystallizing.

Regarding claim 20, as above the insulator layer (166) having lattice plane of (001) that means the lattice plan of insulator layer is parallel to a-axis and b-axis and intersecting of c-axis (a=0, b=0, c=1).

Regarding claims 21, 22, 23, as shown in Lin et al.'s Fig.10G, a layer (169) is considered as a first electrode and the single conductive layer (165) is considered as a second single electrode; the second electrode formed of RuOx (x=2) including a first substance (ruthenium) and a second substance (oxygen).

Regarding claim 24, as discussed in the rejection of claims 21 and 23 above, the dielectric layer (166) having a first compound includes a first substance (Ta) and a second substance (oxygen), the second electrode having a second compound (RuOx) including a trace amount of third substance (ruthenium) and a substantial amount of fourth substance (oxygen).

It is noted that, the second electrode in the device formed by the combination of Lin et al. and Summerfelt et al. is formed of RuOx which is identical as material of second electrode of claimed device. Therefore, it is inherent that RuOx prevent the diffusion of oxygen from the Ta2O5 layer.

Regarding claims 25, 55, Lin et al. teaches that the first electrode (169) is formed of Pt. Lin et al.'s col.9, lines 38-40.

Claim 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kunitomo et al. view of Summerfelt et al. and further in view of Kotectki et al. (US 6,262,450).

Kunitomo et al. and Summerfelt et al. teache all the limitations of claims 1, 3-4, 6, 8-9, 11, and 14-15 as shown above. Kunitomo et al. further teaches that the capacitor structure is formed as an element in a memory cell of a DRAM memory device, wherein the memory device further comprising: a row access circuitry (x0); a column access circuitry (EQ); a controller and an input/output circuit (Kunitomo et al.'s col.10, lines 39-41).

Kunitomo et al. does not explicitly teach that the memory device comprises an address decoder.

Kotectki et al. discloses a DRAM memory device comprises an address decoder. Kotectki et al.'s col.1, lines 30-39.

It would have been obvious to one of ordinary skill in the art to form the DRAM memory device including an address decoder as taught by Kotectki et al. because address decoder is commonly used to form in a peripheral region in order to support the memory device. Kotectki et al.'s col.1, lines 30-39.

Claims 52 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cloud et al. (US 5,815,427) in view of Kunitomo et al. (US 6,235,572) and Summerfelt et al. (US 5,622,893).

Regarding claim 52, Cloud et al. discloses an electronic system comprising: a plurality of circuit modules (memory module, communication module, interconnection module) including a plurality of dies (a first die, a second die, and a third die), wherein the first die including an array of memory cells (10, a DRAM device. Cloud et al.'s abstract and col.4, lines 15-20); a plurality of leads (34, 26, 30) coupled to the plurality of dies to provide unilateral or bilateral communication and control; an user interface (video display, keypad and mouse. Cloud et al.'s col.6, lines 65-67). See Cloud et al.'s Fig.1, and Fig.7.

Cloud et al. does not explicitly teach that the DRAM memory device including an array of memory cells, wherein array of memory cells comprising: a capacitor structure including an insulator having a first compound which including substances, a conductive layer having a second compound including a first substance and a second substance, wherein the second substance in an as-deposited state includes a substantial amount of the second substance so as to inhibit undesired diffusion of at least one substance of the first compound from the insulator layer; at least one transistor having a gate, drain, and source, wherein the drain region is coupled to a second conductive layer.

Kunimoto et al. discloses a semiconductor capacitor structure for storage charge comprising: a metallization layer (a contact plug structure including layer 30 and 49); a single conductive layer (54) formed directly on the metalization layer, the single conductive layer having a compound (ruthenium oxide RuO) including a first substance (Ru) and a second substance (O) is formed by oxidized a Ru layer during crystallization of the tantalum oxide layer (61) (col.20 lines 63-67 and col.21 lines 1-15). Kunitomo et al. Further teaches that the morphology of the semiconductor structure remain stable during the crystallization process (col.20 lines 26-62); a single insulator layer (61, a tantalum oxide layer) formed directly on the single conductive layer, the single insulator layer having a first compound (tantalum oxide); a second conductive layer (62) formed directly on the single insulator layer, wherein the second conductive layer including a conductive portion (a portion of second conductive layer 62 extending on an upper surface of an insulating layer 46) formed below an upper surface of the single conductive layer. See Kunitomo et al.'s Fig.26 and Fig.26.

It would have been obvious to one of ordinary skill in the art to incorporate the DRAM memory device as taught by Kunitomo et al. into Cloud et al.'s electronic system because the capacitor structure and transistor structure of Kunitomo et al.'s DRAM memory has several advantages over conventional DRAM device as following: a capacity insulating film which has heat resistance, less leakage current and high withstand voltage; the film characteristics such as stress of capacity insulating film, surface morphology and density thereof have been improved; the effective film thickness of the transistor's gate insulating film is reduce and the generation of a tunneling is restricted; the performance of the DRAM concerning refresh characteristic has been improved.

Kunitomo et al. does not explicitly teach that the single conductive layer further includes a trace amount of the first substance (ruthenium).

It is conventional and also taught by Summerfelt et al. (col.3 lines 43-55) that the single layer of capacitor electrode is formed by partially or fully oxidized the Ru still provides a stable conductive interface to the HDC material.

It would have been obvious to one of ordinary skill in the art to form the single conductive layer by partially oxidizing the Ru instead of fully oxidizing the Ru layer as taught by Summerfelt et al. because the single conductive layer being formed by both patrially or fully oxidizing Ru layer still provides a stable conductive interface to the HDC material.

It is noted that, the single conductive layer in the device being formed by the combination of Kunitomo et al. and Summerfelt et al. inherently includes a trace amount of the first substance (Ru). It is also noted that the second compound in Kunitomo et al. is identical as the second compound in the claims (ruthenium oxide). So, the second substance (oxygen) in Kunitomo et al. is inherently capable to prevent the oxygen (one substance of insulator layer) form the tantalum oxide (61).

Regarding claim 53, Cloud et al. teach the electronic system is formed in a computer system (80) which further comprising: a processor (44), a monitor (the video display); an output device (88) including a printer; bulk storage devices (90); data, and command buses. Cloud et al.'s Fig.7 and col.7, lines 1-15.

However, Cloud et al. does not explicitly teach that the computer system further comprises a memory controller, a plurality of data links and command links.

It would have been obvious to one of ordinary skill in the art to form the computer system including a memory controller, the data buses including data links, command buses including command signal and command links as claimed because these elements are art recognized elements which are commonly included in a computer system.

Claims 56, 57, 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Summerfelt et al. and further in view of Matsubara et al. (US 6,306,699).

The combination of Lin et al. and Summerfelt et al. teaches all the limitations of claims 1-25 and 54-55 as shown above. However, Lin et al. does not teach that the second conductive layer includes a first conductive portion and a second conductive portion uniformly formed with the first conductive conductive portion, wherein one of the first and second conductive portion is surrounded by a U-shape first single conductive layer.

Matsubara et al. discloses a semiconductor capacitor comprising: a U-shape first single conductive layer (31); a capacitor dielectric layer (21) formed directly on the first single conductive layer; and a second conductive layer (22) formed directly on the dielectric layer, the second conductive layer includes a first conductive portion (a portion of layer 22 on top surface of insulator layer 23) and a second conductive portion (a portion of layer 22 under the to surface of insulator layer 23) uniformly formed with the first conductive conductive portion, wherein the second conductive portion is surrounded by the U-shape first single conductive layer (31). See Matsubara et al.'s Fig.1.

It would have been obvious to one of ordinary skill int the art to incorporate the second conductive layer including the second conductive portion is surrounded by the U-shape first single conductive layer as taught by Matsubara et al. into the device being formed by the combination of Lin et al. and Summerfelt et al. in order to increases capacitive (the effective area) of capacitor structure. Matsubara et al.'s col.1 lines 15-28.

Claims 59-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Summerfelt et al. and further in view of Shimazu et al. (US 6,686,274).

The combination of Lin et al., and Summerfelt et al. teaches all the limitations of claims 1-25, and 54-58 as shown above. However, Lin et al. does not explicitly teach that a silicide region formed over a source/drain (156) where is the contact plug (162) (the metallization layer) contact to.

Shimazu et al. Teaches that a silicide region (9) is formed between a source/drain region (6) and a contact plug (17) to reduce the contact resistance between the contact plug and the source/drain region. See Shimazu et al.'s Fig.5 and col.1 lines 15-22.

It would have been obvious to one of ordinary skill in the art to form the silicide region as taught by Shimazu into Lin et al.'s device in order to reduce the contact resistance between the contact plug and the source/drain region.

Claims 61-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Summerfelt et al., Matsubara et al. and further in view of Shimazu et al. (US 6,686,274).

The combination of Lin et al., Summerfelt et al. and Matsubara et al. teaches all the limitations of claims 1-25, and 54-58 as shown above. However, Lin et al. does not explicitly teach that a silicide region formed over a source/drain (156) where is the contact plug (162) (the metallization layer) contact to.

Shimazu et al. Teaches that a silicide region (9) is formed between a source/drain region (6) and a contact plug (17) to reduce the contact resistance between the contact plug and the source/drain region. See Shimazu et al.'s Fig.5 and col.1 lines 15-22.

It would have been obvious to one of ordinary skill in the art to form the silicide region as taught by Shimazu into Lin et al.'s device in order to reduce the contact resistance between the contact plug and the source/drain region.

The limitations "as-deposited state" in claims 1, 21, 24 and 51-53, "the trace amount of the third substance is oxidized during the crystallization of the dielectric" in claims 24 and 25 are taken to be a product by process limitation, it is the patentability of the claimed product and not of recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Response to Arguments

2. Applicant's arguments with respect to claims 1-25 and 51-63 have been considered but are not persuasive.

Applicants argue that the applied prior art do not teach the conductive layer is formed "directly on" the conductive plug. In response, above rejection clearly pointed out that the conductive layer is formed directly on the conductive plug (it is notice that "directly on" does not mean "directly contact" or "physically contact").

Applicants argue that Lin does not teach the first electrode (the lower capacitor electrode) having a substance in the group as claimed such as Ru. In response, Lin clearly teaches that the lower capacitor electrode (165) is formed of Ru.

Conclusion

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

4. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 872-9306. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

5. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone number is (571) 272-1661. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday.

6. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Eddie Lee who can be reached on (571) 272-1732.

7. Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center Receptionists whose telephone number is 308-0956.

Cuong Nguyen

Primary examiner

10/14/04